XUEYANG LIU

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Education

Georgia Institute of Technology — Atlanta, GA
Ph.D. in Computer Science — *Sept 2021 - Now*

University of Michigan — Ann Arbor, MI
Bachelor of Science in Computer Engineering — *Sept 2018 - May 2020*

Shanghai Jiao Tong University (SJTU) — Shanghai, China
Bachelor of Science in Electronic and Computer Engineering — *Sept 2016 - May 2018*

- Dual degree program at University of Michigan and SJTU

Research Projects

Contention-aware GPU threadblock scheduler for GPU-SSD systems Nov 2022 - Now
Advisor: Prof. Hyesoon Kim *Atlanta, GA*

- Researched heterogeneous systems where GPUs are directly connected to storage; built cycle-lev simulators for such platform by connecting macsim(GPU) and MQSim(SSD) simulators
- Identified SSD contention bottlenecks; evaluated GPU threadblock scheduling algorithms and proposed the new CA-scheduler that accounts for SSD internal property
- Built infrastructure to evaluate large GPU benchmarks including graph and machine learning

Defending contention-based side-channel attack in on-chip networks Sep 2021 - Feb 2022
Advisor: Prof. Hyesoon Kim *Atlanta, GA*

- Customize Garnet from Gem5 to reproduce network contention based attacks
- Implemented mitigation strategies and analyzed performance tradeoff
- CAL 2023: Mitigating Timing-Based NoC Side-Channel Attacks With LLC Remapping

Cross Page Translation Speculation Aug 2019 - Apr 2020
Advisor: Prof. Trevor Mudge *Ann Arbor, MI*

- Proposed speculative Translation Look-aside Buffer (TLB) and nearest-entry TLB translation prediction by exploiting contiguity in physical address allocation
- Profiled and analyzed graph benchmarks using Linux perf on TLB and page table walk performance; customize DynamoRIO memory system simulator for speculative TLB
- SAMOS 2020: CoPTA: Contiguous pattern speculating TLB architecture

Reconfigurable Error Correction Code (ECC) Accelerator Jan 2019 – Apr 2020
Advisor: Prof. Hun-Seok Kim *Ann Arbor, MI*

- Proposed an PE-memory interconnect architecture for general belief propagation ECC algorithms with deterministic control pattern; algorithms include Polar, LDPC and Turbo/Viterbi
- Simulated the architecture in MATLAB and evaluated the bit error rate; implemented in Verilog to evaluate the decoder power, frequency and throughput
- ISLPED 2022:
A Unified Forward Error Correction Accelerator for Multi-Mode Turbo, LDPC, and Polar Decoding

Work Experience

Computing Research Intern Livermore, CA
Lawrence Livermore National Laboratory *May 2023 – Aug 2023*

- Integrated ZHW accelerator into MoSAIC, a heterogeneous tile-based SoC platform at RTL level
- Implemented compression software using MoSAIC APIs; evaluated and optimized date movement between CPU and memory by proposing bew commands
- SC-W 2023:
  Accelerator integration in a tile-based SoC: lessons learned with a hardware floating point compression engine

Systems Technology Research Intern San Jose, CA
Samsung Semiconductor *May 2022 – Aug 2022*

- Studied Samsung's SmartSSD prototype product and designed a performance model to predict the acceleration performance based on device experiments
- Designed and developed a Intel pin tool to divide and profile separate workload regions for offload performance prediction

Hardware Engineer Palo Alto, CA
SambaNova Systems *July 2020 – Aug 2021*

- Designed and optimized hardware assembly for layer normalization on RDU accelerator; integrated the template across software stack
- Updated DDR shim RTL: Adapted DDR4 to dual-channel DDR5; optimized microarchitecture with fine-grain credit management and improved throughput with fifo and arbitration structure
- Automated performance analysis of parallelism in convolution templates with python; analyzed patterns for optimal resource efficiency

Experiences

Graduate Teaching Assistant | *High Performance Computer Architecture* Jan 2025 - May 2025
Graduate Teaching Assistant | *Compiler Design* Jan 2023 - May 2023
Graduate Teaching Assistant | *Processor Design* Jan 2022 - May 2022
Teaching Assistant | *Computer Architecture* Sep 2019 - May 2020
Writing Consultant | *English Writing Center* Aug 2017 - Aug 2018

- Advise SJTU students on writing topics including thesis, structure building and use of language
- Attend weekly training with the consultant group to improve peer communication skills
- Design workshops on writing topics such as database searching

Leadership

Graduate Student Association Mental Health Committee Sep 2023 - May 2024
Chair *Atlanta, GA*

- Led bi-weekly discussions on mental health challenges specific to graduate students and brainstorm on actions
- Connect with directors and staff at Center for Mental Health and Resource(CMHCR) to clarify on-campus resources, seek support for collaborations
- Held mental health town hall meeting in spring 2024, bringing together CMHCR staff and the student body to promote on-campus mental health service and address student questions

Skills

Software Programming Languages: C/C++, Python, Shell, LaTeX, MATLAB, ARM Assembly
Developer Tools: llvm, VS Code, Cadence, Synopsys, Xilinx Vivado/Vitis, Jupyter Notebook